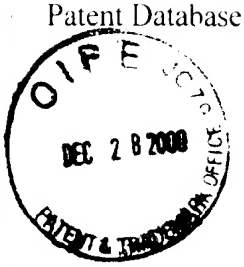

Searching 1996-2000...

Results of Search in 1996-2000 db for:
(("etch stop" AND ACLM/etch) AND ACLM/stop): 610 patents.
*Hits **1** through **50** out of **610***

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Refine Search "etch stop" and ACLM/etch AND ACLM/stop

	PAT. NO.	Title
1	6,159,840	Fabrication method for a dual damascene comprising an air-gap
2	6,159,839	Method for fabricating borderless and self-aligned polysilicon and metal contact landing plugs for multilevel interconnections
3	6,159,792	Method for forming a capacitor of semiconductor device
4	6,159,788	Method to increase DRAM cell capacitance
5	6,159,779	Multi-layer gate for TFT and method of fabrication
6	6,159,385	Process for manufacture of micro electromechanical devices having high electrical isolation
7	6,158,901	Method for the hybrid integration of discrete elements on a semiconductor substrate
8	6,156,643	Method of forming a dual damascene trench and borderless via structure
9	6,154,234	Monolithic ink jet nozzle formed from an oxide and nitride composition
10	6,153,935	Dual etch stop/diffusion barrier for damascene interconnects
11	6,153,541	Method for fabricating an oxynitride layer having anti-reflective properties and low leakage current
12	6,153,527	Semiconductor processing method of making electrical contact to a node received within a mass of insulating dielectric material
13	6,153,521	Metallized interconnection structure and method of making the same
14	6,153,514	Self-aligned dual damascene arrangement for metal interconnection with low k dielectric constant materials and nitride middle etch stop layer
15	6,153,504	Method of using a silicon oxynitride ARC for final metal layer
16	6,150,723	Copper stud structure with refractory metal liner

17 6,150,269 [x] Copper interconnect patterning

18 6,150,230 [x] Trench separator for self-defining discontinuous film

19 6,147,409 [x] Modified multilayered metal line structure for use with tungsten-filled vias in integrated circuit structures

20 6,146,997 [x] Method for forming self-aligned contact hole

21 6,146,954 [x] Minimizing transistor size in integrated circuits

22 6,146,229 [x] Cathode structure for reduced emission and robust handling properties

23 6,144,683 [x] Red, infrared, and blue stacked laser diode array by wafer fusion

24 6,143,657 [x] Method of increasing the stability of a copper to copper interconnection process and structure manufactured thereby

25 6,143,648 [x] Method for forming an integrated circuit

26 6,143,646 [x] Dual in-laid integrated circuit structure with selectively positioned low-K dielectric isolation and method of formation

27 6,143,640 [x] Method of fabricating a stacked via in copper/polyimide beol

28 6,143,602 [x] Methods of forming memory device storage capacitors using protruding contact plugs

29 6,140,755 [x] Actinic radiation source and uses thereofor

30 6,140,705 [x] Self-aligned contact through a conducting layer

31 6,140,238 [x] Self-aligned copper interconnect structure and method of manufacturing same

32 6,140,226 [x] Dual damascene processing for semiconductor chip interconnects

33 6,136,686 [x] Fabrication of interconnects with two different thicknesses

34 6,136,659 [x] Production process for a capacitor electrode formed of a platinum metal

35 6,136,643 [x] Method for fabricating capacitor-over-bit-line dynamic random access memory (DRAM) using self-aligned contact etching technology

36 6,133,635 [x] Process for making self-aligned conductive via structures

37 6,133,144 [x] Self aligned dual damascene process and structure with low parasitic capacitance

38 6,133,140 [x] Method of manufacturing dual damascene utilizing anisotropic and isotropic properties

39 6,133,139 [x] Self-aligned composite insulator with sub-half-micron multilevel high density electrical interconnections and process thereof

40 6,133,129 [x] Method for fabricating a metal structure with reduced length that is beyond photolithography limitations

41 6,130,168 [x] Using ONO as hard mask to reduce STI oxide loss on low voltage device in flash or EPROM process

42 6,127,721 [x] Soft passivation layer in semiconductor fabrication

43 6,127,263 [x] Misalignment tolerant techniques for dual damascene fabrication

44 6,126,311 Dew point sensor using mems

45 6,124,206 Reduced pad erosion

46 6,124,172 Method of making a semiconductor device having source drain structures with self-aligned heavily-doped and lightly-doped regions

47 6,121,073 Method for making a fuse structure for improved repaired yields on semiconductor memory devices

48 6,121,068 Long wavelength light emitting vertical cavity surface emitting laser and method of fabrication

49 6,120,942 Method for making a photomask with multiple absorption levels

50 6,118,508 Liquid crystal displays including reference electrode lines that extend across multiple pixels

Searching 1996-2000...

Results of Search in 1996-2000 db for:
"etch stop": 2365 patents.
*Hits **1** through **50** out of **2365***

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Refine Search "etch stop"

	PAT. NO.	Title
1	6,160,301	Gate structure
2	6,160,296	Titanium nitride interconnects
3	6,160,283	Methods of forming integrated circuitry and integrated circuitry structures
4	6,160,282	CMOS image sensor employing silicide exclusion mask to reduce leakage and improve performance
5	6,159,862	Semiconductor processing method and system using C.sub.5 F.sub.8
6	6,159,857	Robust post Cu-CMP IMD process
7	6,159,840	Fabrication method for a dual damascene comprising an air-gap
8	6,159,839	Method for fabricating borderless and self-aligned polysilicon and metal contact landing plugs for multilevel interconnections
9	6,159,833	Method of forming a contact hole in a semiconductor wafer
10	6,159,822	Self-planarized shallow trench isolation
11	6,159,816	Method of fabricating a bipolar transistor
12	6,159,807	Self-aligned dynamic threshold CMOS device
13	6,159,793	Structure and fabricating method of stacked capacitor
14	6,159,792	Method for forming a capacitor of semiconductor device
15	6,159,788	Method to increase DRAM cell capacitance
16	6,159,786	Well-controlled CMP process for DRAM technology

17 6,159,779 Multi-layer gate for TFT and method of fabrication

18 6,159,385 Process for manufacture of micro electromechanical devices having high electrical isolation

19 6,158,901 Method for the hybrid integration of discrete elements on a semiconductor substrate

20 6,158,845 Ink jet print head having heater upper surface coplanar with a surrounding surface of substrate

21 6,158,384 Plasma reactor with multiple small internal inductive antennas

22 6,157,216 Circuit driver on SOI for merged logic and memory circuits

23 6,157,114 Mechanical signal processor comprising means for loss compensation

24 6,157,081 High-reliability damascene interconnect formation for semiconductor fabrication

25 6,157,078 Reduced variation in interconnect resistance using run-to-run control of chemical-mechanical polishing during semiconductor fabrication

26 6,157,058 Low voltage EEPROM/NVRAM transistors and making method

27 6,157,042 Optical cavity enhancement infrared photodetector

28 6,156,658 Ultra-thin resist and silicon/oxide hard mask for metal etch

29 6,156,643 Method of forming a dual damascene trench and borderless via structure

30 6,156,636 Method of manufacturing a semiconductor device having self-aligned contact holes

31 6,156,615 Method for decreasing the contact resistance of silicide contacts by retrograde implantation of source/drain regions

32 6,156,598 Method for forming a lightly doped source and drain structure using an L-shaped spacer

33 6,156,585 Semiconductor component and method of manufacture

34 6,156,487 Top surface imaging technique for top pole tip width control in magnetoresistive read/write head processing

35 6,156,217 Method for the purpose of producing a stencil mask

36 6,156,149 In situ deposition of a dielectric oxide layer and anti-reflective coating

37 6,155,115 Vibratory angular rate sensor

38 6,154,234 Monolithic ink jet nozzle formed from an oxide and nitride composition

39 6,153,935 Dual etch stop/diffusion barrier for damascene interconnects

40 6,153,905 Semiconductor component including MOSFET with asymmetric gate electrode where the drain electrode over portions of the lightly doped diffusion region without a gate dielectric

41 6,153,901 Integrated circuit capacitor including anchored plug

42 6,153,833 Integrated circuit having interconnect lines separated by a dielectric having a capping layer

43 6,153,541 Method for fabricating an oxynitride layer having anti-reflective properties and low leakage current

44 6,153,527 Semiconductor processing method of making electrical contact to a node received within a mass of insulating dielectric material

45 6,153,523 Method of forming high density capping layers for copper interconnects with improved adhesion

46 6,153,521 Metallized interconnection structure and method of making the same

47 6,153,514 Self-aligned dual damascene arrangement for metal interconnection with low k dielectric constant materials and nitride middle etch stop layer

48 6,153,504 Method of using a silicon oxynitride ARC for final metal layer

49 6,153,495 Advanced methods for making semiconductor devices by low temperature direct bonding

50 6,153,490 Method for forming integrated circuit capacitor and memory